Attorney Docket No.: 026661-004310US
Client Reference No.: ACC-001

PATENT APPLICATION

SIGNAL FLOW DRIVEN CIRCUIT PHYSICAL SYNTHESIS TECHNIQUE

Inventor(s): Pengei Zhang et al.

Assignee: Magma Design Automation, Inc.
1650 Technology Drive
San Jose, CA 95110

Entity: Large

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 925-472-5000

SIGNAL FLOW DRIVEN CIRCUIT PHYSICAL SYNTHESIS TECHNIQUE

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims priority to and the benefit of the filing date of provisional patent application Serial No. 60/442,307 filed Jan. 27, 2003.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates generally to analog layout generation and more specifically it relates to a signal flow driven circuit physical synthesis technique for automatic generation of a high performance and compact layout from a circuit schematic based on signal flow information. The signal flow driven layout methodology is based on two observations: matching and symmetry requirement most critical with devices in the critical signal paths, parasitic reduction (mostly capacitance, resistance, and inductance if possible) is most critical with circuit nodes in the signal path.

[0004] 2. Description of the Related Art

[0005] It can be appreciated that analog layout generation have been in use for years. Typically, analog layout generation are comprised of mostly manual generation of layout, researches in analog/RF layout automation are mostly constraint-driven.

[0006] The main problem with conventional analog layout generation are manual layout is time consuming, error prone and extremely low in productivity. Another problem with conventional analog layout generation are conventional constraint-driven layout automation has not become practical as it is very difficult to generate a set of reasonable constraints. Another problem with conventional analog layout generation are that evaluation of placement or routing solution against certain set of constraints often prohibitively time consuming and computational power hungry.

[0007] While these devices may be suitable for the particular purpose to which they address, they are not as suitable for automatic generation of a high performance and compact layout from a circuit schematic based on signal flow information. The signal flow driven

layout methodology is based on two observations: matching and symmetry requirement most critical with devices in the critical signal paths, parasitic reduction (mostly capacitance, resistance, and inductance if possible) is most critical with circuit nodes in the signal path. The main problem with conventional analog layout generation are manual layout is time consuming, error prone and extremely low in productivity. Another problem is conventional constraint-driven layout automation has not become practical as it is very difficult to generate a set of reasonable constraints. Also, another problem is that evaluation of placement or routing solution against certain set of constraints often prohibitively time consuming and computational power hungry.

[0008] In these respects, the signal flow driven circuit physical synthesis technique according to the present invention substantially departs from the conventional concepts and designs of the prior art, and in so doing provides an apparatus primarily developed for the purpose of automatic generation of a high performance and compact layout from a circuit schematic based on signal flow information. The signal flow driven layout methodology is based on two observations: matching and symmetry requirement most critical with devices in the critical signal paths, parasitic reduction (mostly capacitance, resistance, and inductance if possible) is most critical with circuit nodes in the signal path.

BRIEF SUMMARY OF THE INVENTION

[0009] In view of the foregoing disadvantages inherent in the known types of analog layout generation now present in the prior art, the present invention provides a new signal flow driven circuit physical synthesis technique construction wherein the same can be utilized for automatic generation of a high performance and compact layout from a circuit schematic based on signal flow information. The signal flow driven layout methodology is based on two observations: matching and symmetry requirement most critical with devices in the critical signal paths, parasitic reduction (mostly capacitance, resistance, and inductance if possible) is most critical with circuit nodes in the signal path.

[0010] The general purpose of the present invention, which will be described subsequently in greater detail, is to provide a new signal flow driven circuit physical synthesis technique that has many of the advantages of the analog layout generation mentioned heretofore and many novel features that result in a new signal flow driven circuit physical synthesis

technique which is not anticipated, rendered obvious, suggested, or even implied by any of the prior art analog layout generation, either alone or in any combination thereof.

[0011] To attain this, the present invention generally comprises input module; critical device generator; signal flow driven placement module and parasitic aware routing module. Input module loads circuit netlist, technology files, signal flow information and parasitic constraints. Critical device generator synthesizes circuit component with optimized for matching, symmetry, area and parasitic loading. Placement module places circuit components while optimizing for those in the critical signal flow. Routing module achieves routing for all nets while observing parasitic loading constraints.

[0012] There has thus been outlined, rather broadly, the more important features of the invention in order that the detailed description thereof may be better understood, and in order that the present contribution to the art may be better appreciated. There are additional features of the invention that will be described hereinafter.

[0013] In this respect, before explaining at least one embodiment of the invention in detail, it is to be understood that the invention is not limited in its application to the details of construction and to the arrangements of the components set forth in the following description or illustrated in the drawings. The invention is capable of other embodiments and of being practiced and carried out in various ways. Also, it is to be understood that the phraseology and terminology employed herein are for the purpose of the description and should not be regarded as limiting.

[0014] A primary object of the present invention is to provide a signal flow driven circuit physical synthesis technique that will overcome the shortcomings of the prior art devices. Another object is to provide a signal flow driven circuit physical synthesis technique that generates layout ~~constrains~~ constraints based on signal flow information that is more realistic and practical.

[0015] Another object is to provide a signal flow driven circuit physical synthesis technique that will be a complete system/methodology of placement based on signal flow that allows signal path cells to be placed with high priority.

[0016] Another object is to provide a signal flow driven circuit physical synthesis technique that will be a complete system/methodology of routing based on signal flow that allows critical path to be routed with high priority.

[0017] An object of the present invention is to provide a signal flow driven circuit physical synthesis technique for automatic generation of a high performance and compact layout from a circuit schematic based on signal flow information. The signal flow driven layout methodology is based on two observations: matching and symmetry requirement most critical with devices in the critical signal paths, parasitic reduction (mostly capacitance, resistance, and inductance if possible) is most critical with circuit nodes in the signal path.

[0018] Another object is to provide a signal flow driven circuit physical synthesis technique that automatically synthesizes a physical layout from an existing analog/RF circuit netlist based on critical signal flow path.

[0019] Another object is to provide a signal flow driven circuit physical synthesis technique that generate analog/RF circuit component layout unit based on performance and physical requirement automatically.

[0020] Another object is to provide a signal flow driven circuit physical synthesis technique that achieves analog/RF circuit layout automation with guaranteed circuit performance.

[0021] Another object is to provide a signal flow driven circuit physical synthesis technique that synthesizes the physical layout of analog/RF circuit while observing the critical signal flows, matching and symmetry requirement and parasitic loading constraints.

[0022] Another object is to provide a signal flow driven circuit physical synthesis technique that automatically does circuit cell physical placement and route allowing efficient layout floor planning for analogy/RF circuit automation.

[0023] Other objects and advantages of the present invention will become obvious to the reader and it is intended that these objects and advantages be within the scope of the present invention.

[0024] To the accomplishment of the above and related objects, this invention may be embodied in the form illustrated in the accompanying drawings, attention being called to the fact, however, that the drawings are illustrative only, and that changes may be made in the specific construction illustrated.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Various other objects, features and attendant advantages of the present invention will become fully appreciated as the same becomes better understood when considered in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the several views, and wherein:

[0026] Fig. 1 [[--]] illustrates a flowchart including a Signal Flow Driven Analog/RF Circuit Physical Synthesis Technique ~~Flow Chart~~.

[0027] Fig. 2 [[--]] illustrates a flowchart including a Means of Circuit Performance Assurance, a Means of Physical Layout Floor Planning, and a Means of Incorporating an In-situ Parasitic Extraction Process ~~Flow Chart~~.

DETAILED DESCRIPTION OF THE INVENTION

[0028] Turning now descriptively to the drawings, in which similar reference characters denote similar elements throughout the several views. The attached figures illustrate a signal flow driven circuit physical synthesis technique, which comprises input module; critical device generator; signal flow driven placement module, and parasitic aware routing module. Input module loads circuit netlist, technology files, signal flow information and parasitic constraints. Critical device generator synthesizes circuit component with optimized for matching, symmetry, area and parasitic loading. Placement module places circuit components while optimizing for those in the critical signal flow. Routing module achieves routing for all nets while observing parasitic loading constraints.

[0029] Fig. 1 illustrates a flowchart including a Signal Flow Driven Analog/RF Circuit Physical Synthesis Technique.

[0030] Input module 110 loads circuit netlist 120, technology files, signal flow information 130 (e.g. input rules 140) and parasitic constraints 150. Input module parses the circuit netlist 120 and loads the technology files that necessary for the layout generation. More importantly, it reads in the signal flow information 130 and physical requirement of circuit components and interconnects. Input module 110 can be a graphical user interface that receives user manual input. Input module 110 can be a background reader that takes textual file as input. Input module 110 can be a combination of both user manual input and background data processing tool. Input module 110 can also be a circuit analysis module that automatic generates signal flow information 130 and parasitic constraints 150.

[0031] Critical device generator 160 synthesizes circuit component with optimized for matching, symmetry, area and parasitic loading. Critical device generator 160 synthesizes the physical layout at the unit circuit level while observing matching and loading requirement. Critical device generator 160 can be an integrated part of the physical synthesis tool. Critical device generator 160 can also be a stand-alone tool that employed separately in any analog/RF circuit design flow. Critical device generator 160 can perform on itself with built-in rules. Critical device generator 160 can be driven by requirement generated by automatic circuit analyzer and/or user manual input.

[0032] Placement module 170 places circuit components while optimizing for those in the critical signal flow. The placement module 170 automatically obtains an optimized placement by minimizing the separation of circuit components in the critical signal path to guarantee the performance and by filling in the "voids" with non-critical components to achieve compact layout area. Signal flow driven placement methodology can be employed at circuit component level. Signal flow driven placement methodology can be employed at block level.

[0033] Routing module 180 achieves routing for all nets while observing parasitic loading constraints. Routing module 180 achieves successful routing in 2 steps: it routes first the critical signal flow observing geometry and proximity constraints and then routs all other nets. Routing module 180 can be a grid-based router. Routing module 180 can be grid-less router. Routing module 180 can also incorporate in-situ parasitic extraction.

[0034] The suggested process flow is as follows: input module first loads all input information and other required files, device generator comes into process flow to build all necessary circuit components, next the placement module comes into play and generates the optimized layout placement, finally the routing module completes the physical synthesis by connecting all the nets. Each module can be used separately in other physical design flow. Each module or more than one of these modules can be used in various manners in other design flow.

[0035] Fig. 2 illustrates a flowchart including a Means of Circuit Performance Assurance, a Means of Physical Layout Floor Planning, and a Means of Incorporating an In-situ Parasitic Extraction Process.

[0036] Input information loader 205 reads in the netlist file 210, layout constraints (signal flow information 215, input rules 220, and parasitic constraints 225), and the technology files. The netlist file 210 can be in CDL netlist format or spice netlist file. The layout includes

the place-net constraints and the routing constraints. The technology file can make the layout synthesis tool support different technology. Integrated device generator 230 generates the device layout cell for each device or device combination according to the requirements based on the input netlist. It has the specific considerations for each kind of devices. It will produce the device layout with the best device performance, and reduce the designer's manual work.

[0037] Another device layout source is from the Ecell manager, which provides the interface to access the intellectual property layout cell that makes the layout reuse become possible and speed up the layout synthesis. Because the layout synthesis for the functional block is time consuming so that, the direct use of the layout that was verified before becomes critical. It is also useful to joint-design in a large design group. After the layout cells were prepared, the critical signal path-oriented layout optimizer in steps 235 and 240 does place and route all the cells on the critical signal paths according to the signal flow directions. After the critical signal path was layout, the not critical portion oriented void-filler does place and route all the not critical portion just like void filling to reduce minimize the chip area. Automatic circuit cell physical placement and route also allow efficient layout floor planning for analogy/RF circuit automation.

[0038] In each layout synthesis attempt, the integrated in-situ parasitic extractor is used to evaluate the parasitic effects in step 245. The integrated in-situ parasitic extractor works like a general parasitic extractor, the extracted object is not the whole layout, but the specified nets, the extraction accuracy is also controlled by the parasitic constraints which is generated at the stage of circuit analysis; because the extraction accuracy is changed adaptively and the scope of the extracted layout is specified, the parasitic extraction is speeded up. In step 250, circuit performance assurance may be performed. In step 255, circuit physical layout floor planning may be performed.

[0039] As to a further discussion of the manner of usage and operation of the present invention, the same should be apparent from the above description. Accordingly, no further discussion relating to the manner of usage and operation will be provided.

[0040] With respect to the above description then, it is to be realized that the optimum dimensional relationships for the parts of the invention, to include variations in size, materials, shape, form, function and manner of operation, assembly and use, are deemed readily apparent and obvious to one skilled in the art, and all equivalent relationships to those

illustrated in the drawings and described in the specification are intended to be encompassed by the present invention.

[0041] Therefore, the foregoing is considered as illustrative only of the principles of the invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation shown and described, and accordingly, all suitable modifications and equivalents may be resorted to, falling within the scope of the invention.

61417328 v1